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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,824	09/25/2003	Daniel Alan Brokenshire	AUS920030702US1	7306

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EXAMINER	
NGUYEN, PHILLIP H	
ART UNIT	**PAPER NUMBER**
2191	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,824	BROKENSHIRE ET AL.	
	Examiner	Art Unit	
	Phillip H. Nguyen	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/25/2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2007,2006,2006,2006,2005,2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the original filing date of September 15, 2003. Claims 1-30 are pending and have been considered below.

Note:

2. Regarding to those claims that reciting the phrase "for" or "adapted". They indicate intended use and do not carry any patentable weight. The limitations following the phrase "for" or "adapted" describe only intended use but not necessarily required functionality of the claims. In order for those limitations to be considered, Applicant is required to amend the claims so that the claim limitations are recited in a definite format. For instance, claim 1 recites "A computer-implemented method for loading objects..." can be changed to "A computer-implemented method to load objects..."

3. Applicant appears to invokes 35 U.S.C. 112 6th paragraph in claims 21-23, 25, 27-30 by using "means-plus-function" language. However, Examiner notes that the only "means" for performing these cited functions in the claims appears to be computer product ("software code"). While the claims pass the first of the three prongs test used to determine invocation of paragraph 6, since no other specific functions are disclosed in the specification, the claims do not meet the other tests of the three prongs test. Therefore, 35 U.S.C. 112 6th paragraph has not been invoked when considering these claims below.

Specification

4. The use of the trademark JAVA™ has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Drawings

5. Figures 1-42 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 11 is objected to because of the following informalities: Applicant is required to spell out the letters "DMA" for examining purposes.

Appropriate correction is required.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claim 11 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 17 of copending Application No. 10/670,835. Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications use steps that are clearly similar. For instance, in claim 1, feature (f) of instant application states, "identifying one of the processor to execute a software task, the identification based upon characteristics of the software task and computing resource availability" while the copending application no. 10/670,835 recites, "signal, from the first processor, the second processor". Although, the copending application no. 10/670,835 does not explicitly disclose "identifying one of the processor to execute a software task..." However, it is obvious to

one of ordinary skill in the art to recognize that the processors are identified as first processor and second processor and the second processor is the identified processor that executes (processes) the code (data).

The following tables show few claims to demonstrate the reason for rejection.

Application No. 10/670,824	Application No. 10/670,835
11. An information handling system comprising: a) a plurality of heterogeneous processors; b) a common memory shared by the plurality of heterogeneous processors; c) a first processor selected from the plurality of processors that sends a request to a second processor, the second processor also being selected from the plurality of processors; d) a local memory corresponding to the second processor; e) a DMA controller associated with the second processor, the DMA controller adapted to transfer data between the common memory and the second processor's local memory; and	17. An information handling system comprising: a) a plurality of heterogeneous processors; b) a common memory shared by the plurality of heterogeneous processors; c) a first processor selected from the plurality of processors that sends a request to a second processor, the second processor also being selected from the plurality of processors; d) a local memory corresponding to the second processor; e) a DMA controller associated with the second processor, the DMA controller adapted to transfer data between the common memory and the second processor's local memory; and

f) a loading tool for loading software code to execute on one of the processors, the loading tool including software effective to: i) identifying one of the processor to execute a software task, the identification based upon characteristics of the software task and computing resource availability; ii) loading the software code corresponding to the identified processor into the common memory; and iii) executing the loaded code by the identified processor.	f) a virtual device tool for operating the second processor as a virtual device, the virtual device tool including software effective to: i) signal, from the first processor, the second processor; ii) store data corresponding to the request in the second processor's local; and iii) process the data by the second processor using software code stored in the second processor's local memory.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1, 11, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuoki et al. (United States Patent No.: US 6,526,491 B2).

As per claim 1:

Suzuoki discloses a computer-implemented method for loading objects in a heterogeneous multiprocessor computer system, said method comprising:

- identifying a processor to execute a software task, the identification based upon characteristics of the software task and computing resource availability ("**The number of APUs of a PE assigned to process a particular software cell depends upon the complexity and magnitude of the programs and data within the cell**" Col 3, line 39-42) ;
- loading software code corresponding to the identified processor into shared memory ("**data and applications stored in the shared DRAM**" Col 3, line 34), wherein the shared memory is shared by a plurality of dislike processors that includes the identified processor ("**multiple APUs and multiple PEs sharing the DRAM**" Col 3, line 57-58); and
- executing the loaded code by the identified processor ("**processing a particular software cell**" Col 3, line 40).

As per claim 21:

Recites the same limitations as recited in claim 1 and therefore has been addressed in connection with the rejection set forth to claim 1.

As per claim 11:

Suzuoki discloses an information handling system comprising:

- a plurality of heterogeneous processors ("**four PEs**" Col 8, line 5; **also see FIG. 3**);
- a common memory shared by the plurality of heterogeneous processors ("**Broad bandwidth memory connection 313 provides communication between shared DRAM 315 and these PEs**" Col 8, line 11-13);
- a first processor selected from the plurality of processors ("**PU 203 schedules and orchestrates the processing of data and applications by the APUs**" Col 7, line 59-60; **meaning, PU 203 is selected from a plurality of PUs to schedule and orchestrate the processing of data and application**) that sends a request to a second processor ("**BE bus 1108 provides communication among the PEs**" Col 9, line 51; **meaning, PEs are communicated with each other by signaling**), the second processor also being selected from the plurality of processors ("**PE 201 may be joined or packaged together to provide enhanced processing power**" Col 8, line 2-3; **meaning, PE 201 is a second processor selected from a plurality of PEs**);

- a local memory corresponding to the second processor ("**APU 402 includes local memory 406**" Col 8, line 24);
- a DMA controller associated with the second processor ("**a direct memory access controller (DMCA) 205**" Col 7, line 23) , the DMA controller adapted to transfer data between the common memory and the second processor's local memory ("**DMAC 205 facilitates the transfer of data between DRAM 225 and the APUs and PU of PE 201**" Col 7, line 51-52);
- a loading tool for loading software code to execute on one of the processors (**reading of data from the shard DRAM**" Col 3, line 55-56), the loading tool including software effective to:
    - identifying one of the processors to execute a software task, the identification based upon characteristics of the software task and computing resource availability ("**The number of APUs of a PE assigned to process a particular software cell depends upon the complexity and magnitude of the programs and data within the cell**" Col 3, line 39-42; **meaning, processors are mapped to software cells to determine a particular processor for each software cell**)
    - loading the software code corresponding to the identified processor into the common memory (**reading of data from the shard DRAM**" Col 3, line 55-56); and

- executing the loaded code by the identified processor ("**processing a particular software cell**" Col 3, line 40).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2-9, 12-19, and 22-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki et al. (United States Patent No.: US 6,526,491 B2).

As per claim 2:

Suzuoki discloses the method as in claim 1 above, but does not explicitly discloses:

- prior to the identifying, compiling a source program into at least two object files, each **adapted to** be executed on a different processor selected from the plurality of dislike processors, wherein the software code that is loaded and executed is one of the object files.

However, Suzuoki discloses ("**The code fro the applications preferably is based upon the same common instruction set**" Col 3, line 13-14). It would have been obvious to one having an ordinary skill in the art at the time the invention was made to recognize that processors understand only instruction set not source code.

Therefore, one of ordinary skill in the art would have know that prior processing the instruction set of the software cell, the source program must be compiled into object file(s) and producing instruction set for processing by the processors.

As per claim 3:

Suzuoki discloses the method as in claim 2 above; and further discloses:

- analyzing the source program for program characteristics ("**Each software cell preferably contains a global identification (global ID) and information describing the amount of computing resources required for the cell's processing**" Col 3, line 14-17; **meaning, source code of each application has been analyzed and stored with the application in each software cell**); and
- storing the program characteristics ("**data and applications stored in the shared DRAM**" Col 3, line 34).

As per claim 4:

Suzuoki discloses the method as in claim 3 above; and further discloses:

- wherein at least one of the program characteristics is selected from the group consisting of data locality, computational intensity, and data parallelism ("**The APUs perform this processing in a parallel and independent manner**" Col 3, line 32; **since the processors process data and application in parallel,**

therefore, the program characteristic must be selected from data parallelism).

As per claim 5:

Suzuoki discloses the method as in claim 4 above, but does not explicitly discloses wherein identifying the processor further comprises:

- retrieving the program characteristics;
- retrieving current system characteristics, wherein the current system characteristics includes processor load characteristics for the plurality of dislike processors; and
- combining the program characteristics and the currently system characteristics to determine which of the dislike processors to assign the software task.

However, Suzuoki discloses ("**The number of APUs of a PE assigned to processing a particular software cell depends upon the complexity and magnitude of the programs and data within the cell**" Col 3, line 38-42).

Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to recognize that retrieving the program characteristics from the cell and the characteristics for each processor must be performed. Further more, comparison or mapping or combining must also be performed in order to assign the APUs of PE to a particular software cell for processing data and applications.

As per claim 6:

Suzuoki discloses the method as in claim 5 above; and further discloses:

- wherein at least one of the current system characteristics is selected from the group consisting of processor availability for each of the dislike processors, and a data size of data being processed by the software task ("**depends upon the complexity and magnitude of the program and data within the cell**" Col 3, line 41).

As per claim 7:

Suzuoki discloses the method as in claim 1 above; and further discloses:

- determining that the identified processor has a scheduler for scheduling tasks for the processor ("**the PU schedules and orchestrates the processing**..." Col 3, line 29; **PU is a scheduler**); and
- scheduling the software code to execute on the identified processor ("**the PU schedules and orchestrates the processing of data and applications by the APUs**" Col 3, line 29-30).

Suzuoki does not explicitly discloses the scheduling including:

- writing a software code identifier corresponding to the software code to a run queue corresponding to the identified processor.

However, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to recognize that in order for scheduling tasks, a

system needs a queue for storing tasks or global ID of each software cell corresponding to a particular processor in the order in which a particular processor executes them.

As per claim 8:

Suzuoki discloses the method as in claim 1 above; and further discloses:

- signaling the identified processor ("**BE bus 1108 provides communication among the PEs of BE 1102**" Col 9, line 51; **meaning, a communication is provided among PEs for signaling each other**);
- reading, by the identified processor, the software code from the shared memory into a local memory corresponding to the identified processor ("**APU's reading of data from and the write of data to the shared DRAM**" Col 3, line 55-56); and
- executing the software code by the identified processor ("**processing a particular software cell**" Col 3, line 40).

As per claim 9:

Suzuoki discloses the method as in claim 8 above; and further discloses:

- writing an instruction block in the shared memory ("**DMAC 1412 reads and writes blocks of data containing 1024 bits**" Col 11, line 5), the instruction block including the address of the loaded software code and the address of an input buffer ("**storing and accessing the smallest addressable memory unit of a DRAM, e.g., a block of 1024 bits**" Col 11, line 2-3); and

- reading the software code and the input buffer from the locations identified in the instruction block to the identified processor's local memory ("**DMAC 1412 reads and writes blocks of data containing 1024 bits**" Col 11, line 5; **DMAC is a local memory of a processor**).

As per claims 12-19 and 22-29:

- these are system claims and computer product claims, recite the same limitations as recited in claims 2-9, and therefore, have been addressed in connection with the rejection set forth to claims 2-9.

13. Claims 10, 20, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki et al. (United States Patent No.: US 6,526,491 B2), in view of Fiacconi et al. (United States Patent No.: 4,862,354).

As per claim 10:

Suzuoki discloses the method as in claim 9 above; and further discloses:

- signaling the identified processor from one of the other processors ("**BE bus 1108 provides communication among the PEs of BE 1102**" Col 9, line 51);
- reading, by the identified processor, the instruction block in response to the signal ("**DMAC 1412 reads and writes blocks of data containing 1024 bits**" Col 11, line 5).

Suzuoki does not explicitly discloses:

- writing the address of the instruction block to a mailbox that corresponds to the identified processor.

However, Fiacconi discloses an analogous method that using mailbox in a shared memory to provide a communication between processors ("**to provide communications through mailboxes in a shared memory which can be accessed by several processors**" Col 1, line 57-58).

Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify Suzuoki's approach to include mailbox to provide communication between processors. One of ordinary skill in the art would have been motivated to modify because by using mailbox, processor can communicate with each other by writing messages into the mailbox ("**Thus, a processor A, if it wants to communicate with a processor B, simply writes a message into the mailbox for processor B**" Col 1, line 62-64).

As per claims 20 and 30:

- recite the same limitations as recited in claim 10 above, and therefore, have been addressed in connection with the rejection set forth to claim 10.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip H. Nguyen whose telephone number is (571)

270-1070. The examiner can normally be reached on Monday - Thursday 10:00 AM - 3:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PN
02/09/2007

WEI ZHEN
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